

## IN THE CLAIMS

1. (Canceled)
2. (Canceled)
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15. (Currently amended) A system for converting an input voltage VIN to a digital

output, comprising: K linear flash-type analog-to-digital (A/D) converter apparatuses  $Z_1, Z_2, \dots, Z_K$  respectively characterized by reference voltage step sizes  $\Delta V_1, \Delta V_2, \dots, \Delta V_K$  and respectively adapted to convert  $V_{IN}$  into multibit strings  $S_1, S_2, \dots, S_K$ , wherein  $\Delta V_1 < \Delta V_2 < \dots < \Delta V_K$ , and wherein K is greater than or equal to 2; and encoder means for ~~applying a scale factor to~~ multiplying or dividing at least a selected one of  $S_1, S_2, \dots, S_K$  by a value to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within  $S_1, S_2, \dots, S_K$ .

16. (Previously presented) The system of claim 15, wherein  $S_1, S_2, \dots, S_K$  each have a same number of bits.

17. (Previously presented) The system of claim 15, wherein  $S_1, S_2, \dots, S_K$  do not each have a same number of bits.

18. (Previously presented) The system of claim 15, wherein for  $k=1, 2, \dots, K$  the A/D converter apparatus  $Z_k$  comprises an arithmetic unit  $A_k$  in series with an A/D converter  $B_k$ , wherein the A/D converters have a same working voltage range, wherein  $V_{IN}$  is within the working voltage range, wherein the working voltage range comprises K contiguous voltage subranges denoted as  $\delta V_1, \delta V_2, \dots, \delta V_K$  in order of lower to higher voltages, wherein for  $k=1, 2, \dots, K$  the arithmetic unit  $A_k$  is adapted to change  $V_{IN}$  into a new input voltage  $V_{IN,k}$  in accordance with a transformation of  $\delta V_k$  into the working voltage range and A/D converter  $B_k$  is adapted to transform  $V_{IN,k}$  into the multibit string  $S_k$ .

19. (Previously presented) The system of claim 18, wherein  $\delta V_1, \delta V_2, \dots, \delta V_K$  have values such the error of the digital output relative to  $V_{IN}$  is a piecewise continuous function of  $V_{IN}$  within the working voltage range, said piecewise continuous function of  $V_{IN}$ , the piecewise continuous function having K pieces, wherein the relative error within each said piece of the K pieces is a monotonically decreasing function of  $V_{IN}$ , and wherein each piece of the K pieces has about a same maximum relative error.

20. (Previously presented) The system of claim 15, wherein  $K=2$ , wherein the A/D converter apparatuses Z1 and Z2 comprise A/D converters B1 and B2 having working voltage ranges  $\delta_1$  and  $\delta_2$ , respectively, such that  $\delta_2$  is a subset of  $\delta_1$  and  $\delta_2/\delta_1$  is an integer subject to  $\delta_2/\delta_1 > 1$ , wherein B1 and B2 are respectively adapted to convert VIN to S1 and S2, and wherein the encoder means is adapted to generate the digital output as S2 if S2 is not within the voltage range  $\delta_1$  else the encoder means is adapted to generate the digital output as S1 multiplied by  $\delta_2/\delta_1$ .
21. (Previously presented) The system of claim 20, wherein  $\delta_2/\delta_1 = 2J$ , and wherein J is a positive integer.
22. (Currently amended) A method for converting an input voltage VIN to a digital output, comprising: providing K linear flash-type analog-to-digital (A/D) converter apparatuses Z1, Z2, ..., ZK respectively characterized by reference voltage step sizes  $\Delta V_1, \Delta V_2, \dots, \Delta V_K$ , wherein  $\Delta V_1 < \Delta V_2 < \dots < \Delta V_K$ , and wherein K is greater than or equal to 2; converting VIN, by converter apparatuses Z1, Z2, ..., ZK, into multibit strings S1, S2, ..., SK, respectively; and multiplying or dividing at least a selected one of combining S1, S2, ..., and SK by a value to generate the digital output, wherein the digital output has a sufficient number of bits to preserve the accuracy that is contained within S1, S2, ..., and SK.
23. (Previously presented) The system of claim 22, wherein S1, S2, ..., and SK each have a same number of bits.
24. (Previously presented) The method of claim 22, wherein S1, S2, ..., and SK do not each have a same number of bits.
25. (Previously presented) The method of claim 22, wherein for  $k=1, 2, \dots, K$  the A/D converter apparatus Zk comprises an arithmetic unit Ak in series with an A/D converter Bk, wherein the A/D converters have a same working voltage range, wherein VIN is

within the working voltage range, wherein the working voltage range comprises  $K$  contiguous voltage subranges denoted as  $\delta V_1, \delta V_2, \dots, \delta V_K$  in order of lower to higher voltages, said method further comprising: changing  $V_{IN}$  by the arithmetic unit  $A_k$  for  $k=1, 2, \dots, K$ , into a new input voltage  $V_{IN,k}$  in accordance with a transformation of  $\delta V_k$  into the working voltage range; and transforming  $V_{IN,k}$  by the A/D converter  $B_k$ , into the multibit string  $S_k$ .

26. (Previously presented) The method of claim 25, wherein  $\delta V_1, \delta V_2, \dots, \delta V_K$  have values such the error of the digital output relative to  $V_{IN}$  is a piecewise continuous function of  $V_{IN}$  within the working voltage range, said piecewise continuous function of  $V_{IN}$ , the piecewise continuous function having  $K$  pieces, wherein each two consecutive pieces of the  $K$  pieces are discontinuously joined together, wherein the relative error within each said piece of the  $K$  pieces is a monotonically decreasing function of  $V_{IN}$ , and wherein each piece of the  $K$  pieces has about a same maximum relative error.

27. (Previously presented) The method of claim 22, wherein  $K=2$ , wherein the A/D converter apparatuses  $Z_1$  and  $Z_2$  comprise A/D converters  $B_1$  and  $B_2$  having working voltage ranges  $\Delta_1$  and  $\Delta_2$ , respectively, such that  $\delta_2$  is a subset of  $\delta_1$  and  $\delta_2/\delta_1$  is an integer subject to  $\delta_2/\delta_1 > 1$ , wherein  $B_1$  and  $B_2$  are respectively adapted to convert  $V_{IN}$  to  $S_1$  and  $S_2$ , and wherein said combining includes generating the digital output as essentially  $S_2$  if  $S_2$  is not within the voltage range  $\delta_1$  else said combining includes generating the digital output essentially as  $S_1$  multiplied by  $\delta_2/\delta_1$ .

28. (Previously presented) The method of claim 27, wherein  $\delta_2/\delta_1 = 2J$ , and wherein  $J$  is a positive integer.